SUBCONTRACT TITLE**:** **FABRICATION AND PHYSICS OF CDTE DEVICES BY SPUTTERING**

SUBCONTRACT NO**: RXL-5-44205-01**

QUARTERLY TECHNICAL STATUS REPORT FOR**: Phase 1/Quarter 2**

SUBMITTED TO**:** **Ken Zweibel**
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This progress report covers the second quarter of Phase 1 for the period June 1, 2005, through August 31, 2005, of the above Thin Film Photovoltaic Partnership Program subcontract. During this quarter we worked on spatial and temporal variations in electronic transport through a CdTe-based Schottky barrier, ellipsometric diagnostics, device physics modeling, and thin CdTe solar cell limitations. In this report we highlight our recent results on optical spectroscopy of deep levels in CdTe single crystal (task 1.3.1) and analysis of structural evolution during growth of CdS and CdTe from real time spectroscopic ellipsometry (task 1.3.2).

Task 1.3.1 Photoluminescence Identification of Phosphorus in CdTe Single Crystals

Photoluminescence is convenient and powerful method to probe the material properties of an operating solar cell and to investigate the defect states in the active semiconductor material. PL is particularly convenient for studies of the junction region. However, the unambiguous identification of the transitions responsible for the light emission, particularly in polycrystalline thin films has been elusive. Partly to address this difficulty of identification, we have started a series of measurements on single crystals which have received calibrated doses of known atoms from ion implantation since 2001. The disadvantage of ion implantation is that large numbers of defects are created, typically 1000 displacements for each atom implanted. Earlier we used Te-implanted crystalline CdTe to show that with a proximity cap, 400°C annealing in nitrogen allowed the implantation-induced damage to be removed.

In this phase of the study, we prepared phosphorus-implanted CdTe crystals for PL. CdTe wafers supplied by Nikko Material Co[1] were used. P ions with three kinetic energies of 350, 160 and 70 keV were implanted. To achieve a final uniform P profile below the wafer surface, we selected 81.30, 17.89 and 0.81% of the total ion amount for the three energies, respectively, as indicated by Monte Carlo simulations in SRIM. The ion concentration profile generated by SRIM has been plotted in Fig. 1. The projected range R_p and the range straggling ΔR_p from the simulation are respectively 0.284 and 0.159 μm. The average amount of vacancies calculated to be generated by ion bombardment is 1792 v*acancies/ion*.

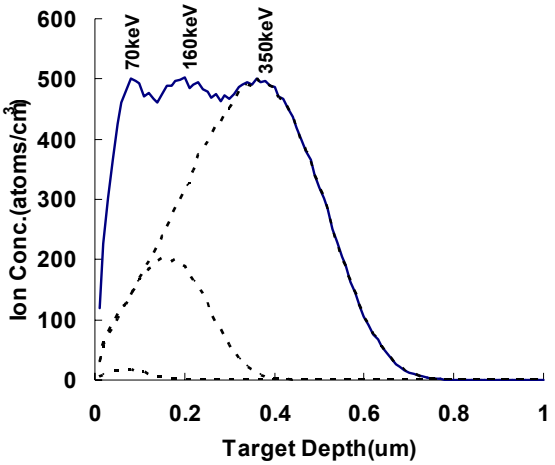

Fig. 1 **Simulated P atom distribution profile in CdTe after (solid line) 350, 160 and 70 keV implantation into same target with 5×10^5, 1.1×10^5 and 5×10^3 P ions respectively, and (dashed line) same amount of P ions for each energy but individually implantation.**

The P species implanted into the CdTe crystal are then assumed to be uniformly distributed from the surface to a depth of $R_p + \Delta R_p$. The crystals were implanted with three different P concentrations: 1×10^{15}, 1×10^{16}, 1×10^{17} (cm^{-3}) with the triple energy protocol described above. Implantation was achieved at the Toledo Heavy Ion Accelerator Lab in the Department of Physics and Astronomy at The University of Toledo. *Red phosphorus* powder was vaporized in the high vacuum chamber of the accelerator as the ion source for implantation. CdTe wafers were cut from the same piece to avoid any crystal structure or impurity variations. Standard annealing, at 400 °C for 30 minutes in N_2 with the proximity cap of polycrystalline CdTe film, was carried out before PL.

After the implantation, all three P-implanted wafers were etched in 0.05% Br methanol solution for 5 seconds to remove any possible surface defects introduced by the manufacturer's surface polish. This process has been measured to remove only 45Å CdTe on the surface.

Power-dependent PL of P-implanted CdTe was carried out with excitation at the 488nm line of the Ar^+ ion laser with the sample temperature around 40 K. Phosphorus concentration-dependent features have been identified as represented in Fig. 2.

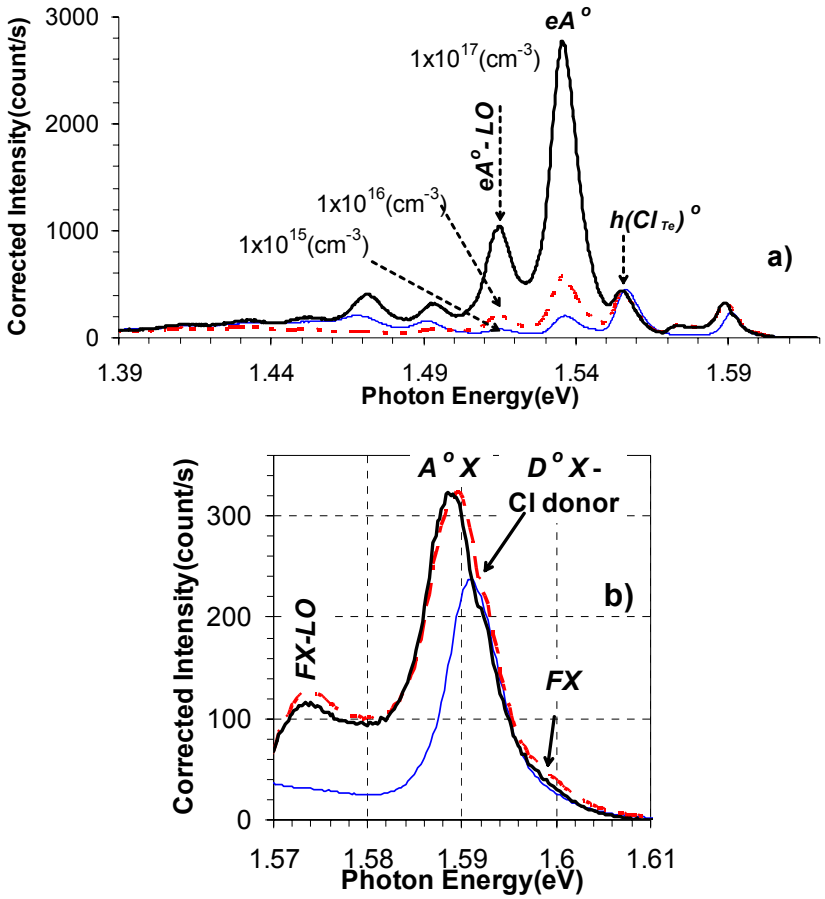

Fig. 2 **a) PL of P-implanted 2nd quality NM CdTe crystal with P concentration of $1x10^{15}$, $1x10^{16}$, $1x10^{17}$(cm^{-3}), and b) spectra in excitonic band range. PLs were excited with 488nm laser beam focused to power density 11.7W/cm^2. Samples were cooled down to approximately 40 K.**

A free-to-bound emission at 1.556 eV corresponding to transitions of holes in the valence band to intrinsic Cl donors in the CdTe wafer, reported in the MRS Spring conference 2005,[1] is observed in the spectra, as shown in Fig. 2a. The intensities of this emission line do not depend on phosphorus concentration.

A transition at ~1.536 eV also appears in the P-implanted CdTe crystal (Fig. 2a). It is easily confused with the phonon replica of the 1.556 eV Cl-related free-to-bound emission, which may also appear at 1.536 eV. However, the intensities of this emission line and its phonon replica at ~ 1.515 eV are observed to depend on phosphorus concentration in the samples, as shown in Fig. 2a. We have identified the asymmetric shape of this 1.536 eV line and fitted it with the *free-to-bound* transition model proposed by D. M. Eagles in 1960.[2] This *free-to-bound* transition most likely corresponds to electrons in the conduction band recombining with holes on a neutral acceptor state (eA^o) of phosphorus on the tellurium site (P_{Te}^o).

Eagles's free-to-bound transition model was employed to fit the electron-to-P-acceptor transition lines as shown in Fig. 3. The best fitting gives an electron temperature T_e = 48 K with the

activation energy of E_I = 70.6 meV. The computation with peak energy (E_{peak} = 1.5355 eV) and bandgap (E_g = 1.604 eV) also gives:

$$E_I = E_g - E_{peak} + KT_e/2 = \mathbf{69\ meV}.$$

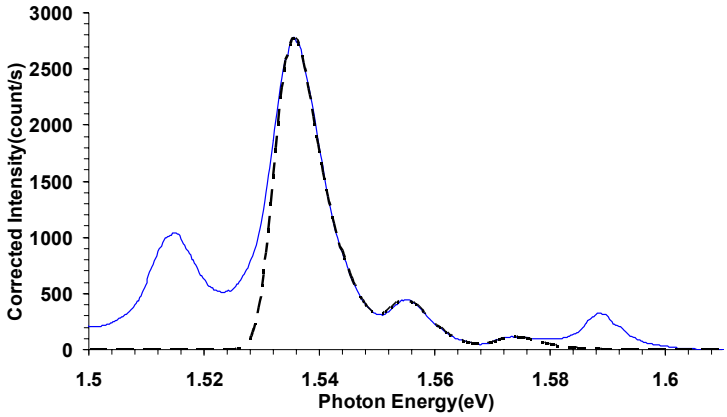

Fig. 3 **Fitting to conduction band to P acceptor (eA^0 at 1.5355 eV) and valence band to intrinsic Cl donor (hD^0 at 1.556 eV) transitions with Eagles's model of free-to-bound transition line shape. Solid line: experimental PL spectrum of CdTe: P 1x10^{17} (cm^{-3}) excited by 11.7W/cm^2 488nm. Broken line: model.**

In the excitonic region, an acceptor-bound exciton recombination line peak at 1.588~1.589 eV (see Fig. 2b) is observed. The shoulder at approximately 1.592 eV can be understood as the Cl-donor-bound exciton recombination.[1]

A temperature-dependent PL intensity study was carried out on the same phosphorus-implanted wafers. PL spectra were collected in the temperature range from T = 8.6 to 120 K. Samples were cooled down by the liquid He refrigerator to 8.6 K and then gradually heated up with temperature steps of 3, 5 or 10 degrees depending on how rapidly the PL features varied with temperature. Spectra were excited by 488 nm laser with power density of 560 (mW/cm^2) (5.6 suns).

The slope of the high temperature end of the Arrhenius plot can provide the activation energy of the impurity. For convenience in comparing the absolute line intensities of different phosphorus concentrations, *log[I(T)]* is used for the ordinate in the Arrhenius plot, instead of *log[I(T)/I(0)]* as usual. As represented in Fig. 4, intensities of the conduction-band-to-P-acceptor transition at ~1.536 eV of the samples with three different P concentrations are fitted with the single-activation-energy model.

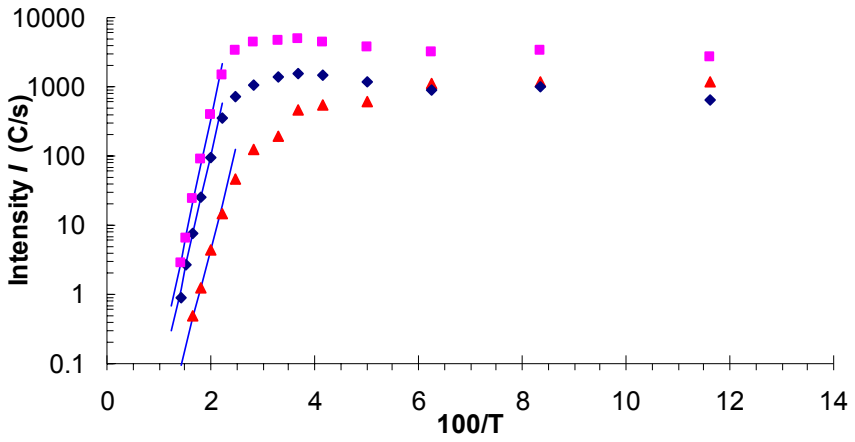

Fig. 4 **Arrhenius plot of temperature dependence of conduction-to-P-acceptor (eA^o) line intensity at 1.536 eV and fitting to $C \cdot exp(E_1/KT)$.**

Fitting of the high temperature side to an $exp(E_i/KT)$ curve in the Arrhenius plot indicates that the activation energies of the electron-to-P-acceptor line in the three P-implanted CdTe crystals apparently *increase* with phosphorus concentration, as summarized in Table 1. Fairly close activation energies have been obtained for the two higher P concentration samples ($1x10^{16}$ and $1x10^{17}$ (cm^{-3})). The energies are 67.8 and 72.0 meV respectively. However the sample with the lowest P concentration $1x10^{15}$ (cm^{-3}) yields E_A = 58.2 meV, which is significantly different from the other two. We do not fully understand this discrepancy.

Table 1 **Activation energy of electron-to-acceptor depending on P concentrations.**

P concentration (cm^{-3})	Activation Energy (meV)	Peak Position (eV) at T =8.6 K
$1x10^{17}$	72.0 ± 0.8	1.539
$1x10^{16}$	67.8 ± 1.6	1.539
$1x10^{15}$	58.2 ± 1.2	1.538

In 1983, E. Molva et al identified the ionization energy of the ground and first excited state of P acceptor in CdTe at 68.2 and 17.3 meV.[3] They calculated the ionization energy of the phosphorus acceptor based on observations of electron-to-acceptor eA^o peak energy. In our study, fitting to the high temperature side of the Arrhenius plot confirms the shallow P acceptor level in CdTe with ground energy level approximately 69 meV above the valence band (E_v + 69 meV) although there may be some dependence on phosphorus concentration.

This study indicates that P can serve as a shallow acceptor in CdTe, although we have not yet determined the electrically active fraction. The challenge is to find a suitable method for introducing the phosphorous into electrically active sites in *polycrystalline* CdTe and maintaining that activity through the stages of cell processing.

Task 1.3.2. Analysis of Structural Evolution during Growth of CdS and CdTe from Real Time Spectroscopic Ellipsometry

The first quarterly report of Phase I described ex situ spectroscopic ellipsometry (SE) studies of CdTe layers incorporated into superstrate solar cells. In these studies, it was shown how the optical properties can be obtained through the depth of the CdTe layer from experiments in which Br_2/methanol etching is used to reduce the CdTe thickness step-by-step and SE is used for optical/structure analysis after each etching step. These optical properties in turn provide information on depth profiles in the void structure and grain size. These experiments were performed using $CdCl_2$-treated solar cell structures without the back contact; so, in the interpretation of the results, one obtains insights into the combined effects of deposition and treatment that lead to the measured structural profiles of the CdTe layers.

In this quarter, research efforts have concentrated on the structural evolution of the CdTe layers during deposition, and in the second phase, the role of the $CdCl_2$ treatments will be explored. Figure 5(a) shows optical calculations of the effect of different volume fractions of uniformly distributed voids on the dielectric function of bulk single crystal CdTe from the literature [4], whereas Fig. 5(b) shows the effect of surface roughness layers of different thicknesses on the pseudo-dielectric function of the three-medium structure (ambient/roughness/bulk). (The pseudo-dielectric function is calculated assuming a single interface between the ambient and a hypothetical bulk layer.) Figure 5(c) shows the effect of

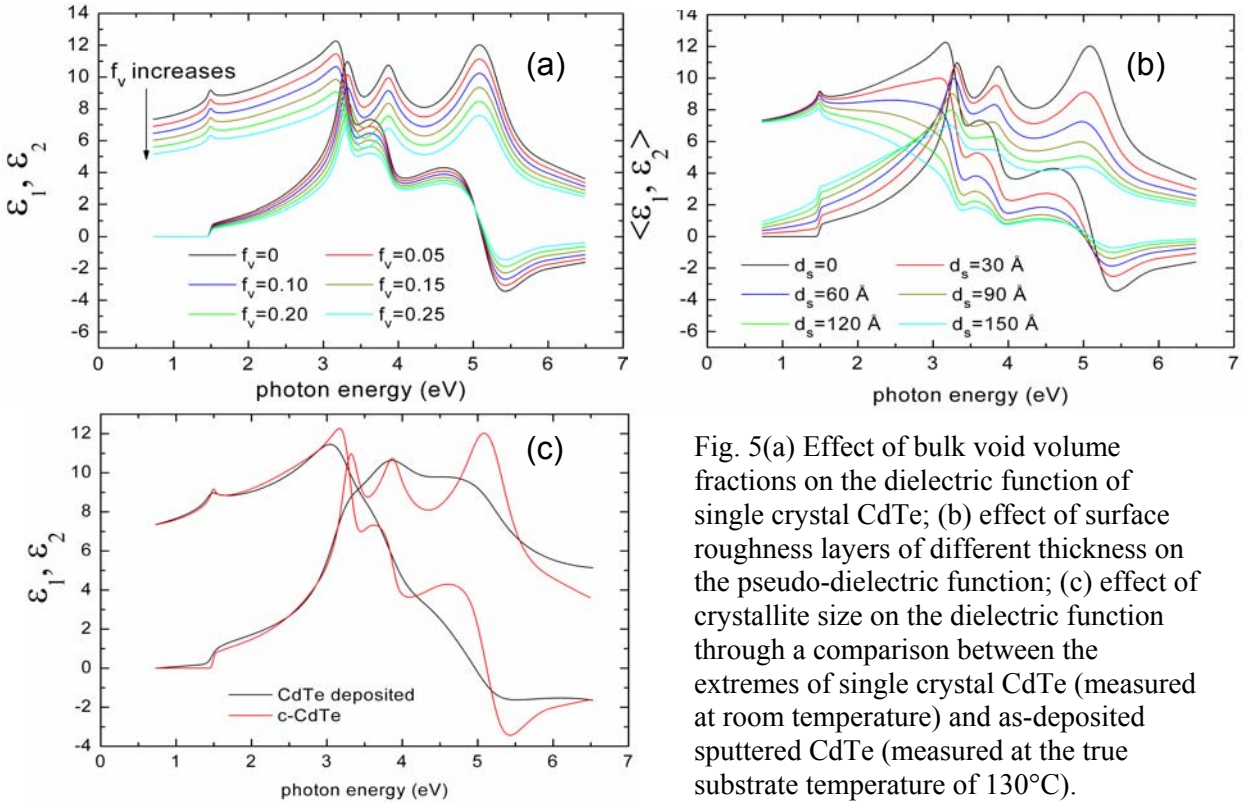

Fig. 5(a) Effect of bulk void volume fractions on the dielectric function of single crystal CdTe; (b) effect of surface roughness layers of different thickness on the pseudo-dielectric function; (c) effect of crystallite size on the dielectric function through a comparison between the extremes of single crystal CdTe (measured at room temperature) and as-deposited sputtered CdTe (measured at the true substrate temperature of 130°C).

crystallite size on the dielectric function through a comparison between the extremes of single crystal CdTe (measured at room temperature [4]) and as-deposited sputtered CdTe (measured at the true substrate temperature of 130°C), the latter being a fine-grained polycrystalline material. A comparison of the different trends in Fig. 5 shows that it is easy to distinguish the three effects of voids, roughness, and grain size as long as a sufficiently wide spectral range is studied.

Figure 6 shows the surface roughness evolution with bulk layer thickness during the nucleation and coalescence of five CdTe films prepared by magnetron sputtering onto c-Si substrates at different nominal substrate temperatures. For this series, the Ar sputtering gas pressure and the rf plasma power were fixed at 18 mTorr and 60 W, respectively. The nominal substrate temperature is obtained using a thermocouple mounted in the heating assembly above the substrate holder, a configuration that enables continuous substrate rotation, but requires careful calibration to determine the true substrate temperature. In all cases, graphite cloth was used between the substrate and its holder, which ensures that the nominal and true substrate temperatures are close to one another for these depositions. For each deposition, the plasma and gas flow were terminated in two steps after a thickness near 500 Å, in order to evaluate the separate effects of the plasma and sputtering gas on the substrate temperature calibration. These results along with the procedure to determine the true substrate temperature from the nominal value will be reported separately. The plasma/(gas flow) termination steps generate a monolayer

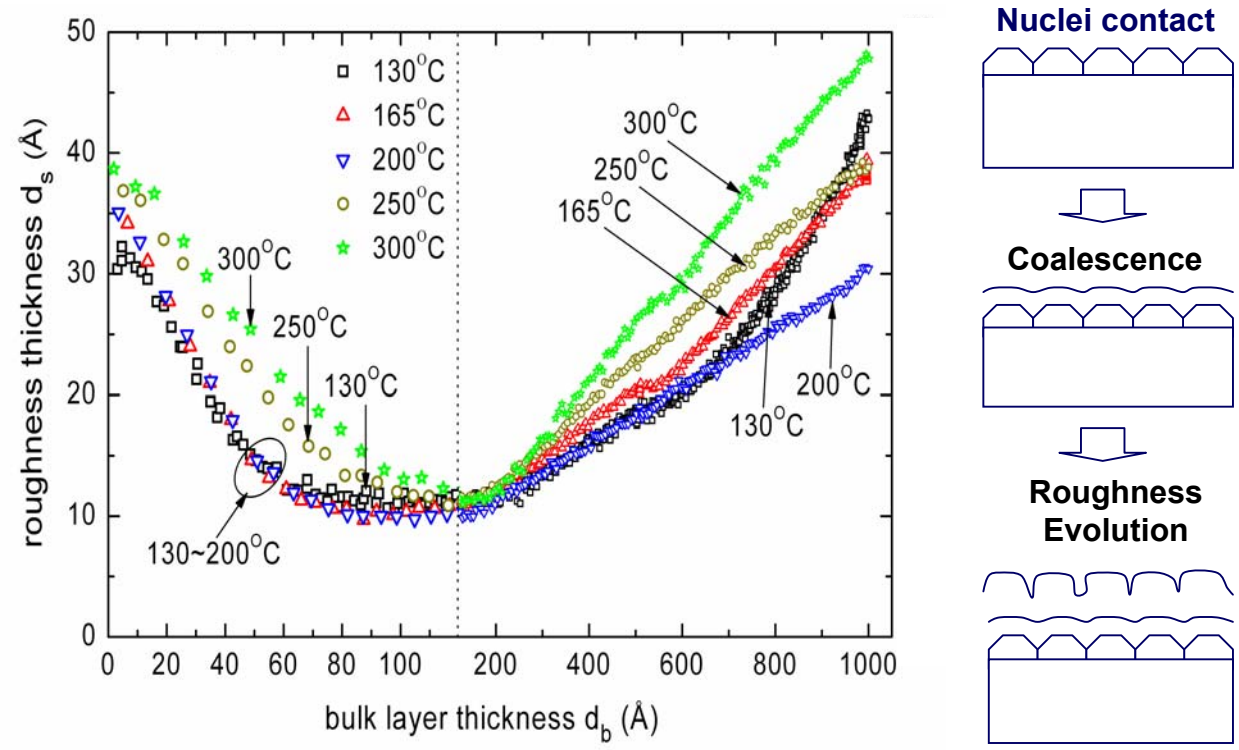

Fig. 6: Surface roughness layer thickness versus bulk layer thickness for CdTe films prepared at different (nominal) substrate temperatures during nuclei coalescence in the first 120 Å of bulk layer thickness and over the range from 120 to 1000 Å in bulk layer thickness. (Note the scale change at d_b=120 Å.)

level feature in the data of Fig. 6, but does not appear to change the overall trends in the roughness evolution. A second plasma stop/restart step is performed after 1000 Å. During this step, the sample is cooled to room temperature for a measurement of the optical properties of the CdTe prepared at the different temperatures. The reason for this step is to provide a comparison of the room temperature optical properties of these layers before the complex structural evolution is built into the sample, making the analysis more difficult and less certain.

Interesting trends can be noted in Fig. 6. First, the thickness at which the nuclei make contact increases with increasing temperature. This indicates a reduction in the nucleation density with increasing temperature. This in turn indicates either: (i) a lower density of nucleation sites at higher temperature for the case in which nucleation is controlled by substrate defects, or (ii) a higher diffusion length of film precursors on the substrate for the case in which nucleation is controlled by the random aggregation of critical-sized clusters. Coalescence occurs to the same roughness thickness of ~12 Å, irrespective of the nominal substrate temperature. For all depositions, roughening begins just after coalescence, starting from a thickness of ~200 Å. The surface roughness thickness tends to increase linearly with bulk layer thickness for substrate temperatures of 200°C and above. At lower temperatures, roughening tends to occur super-linearly; this effect is noted most clearly for the lowest substrate temperature deposition (130°C). The origin of these trends becomes clearer when the overall structural evolution is characterized, including void fraction development. From Fig. 6 it is interesting to note that the deposition at 200°C exhibits the slowest roughness increase above 200 Å.

Figure 7(a) shows the real and imaginary parts of the dielectric function for the five CdTe films deposited at the different temperatures. All these results were obtained at room temperature, at a thickness of ~1000 Å, and after stopping the deposition temporarily and cooling the sample from the deposition temperature. For this deposited thickness, the void volume fraction, as indicated by the reduced amplitude of the dielectric function, increases monotonically with increasing

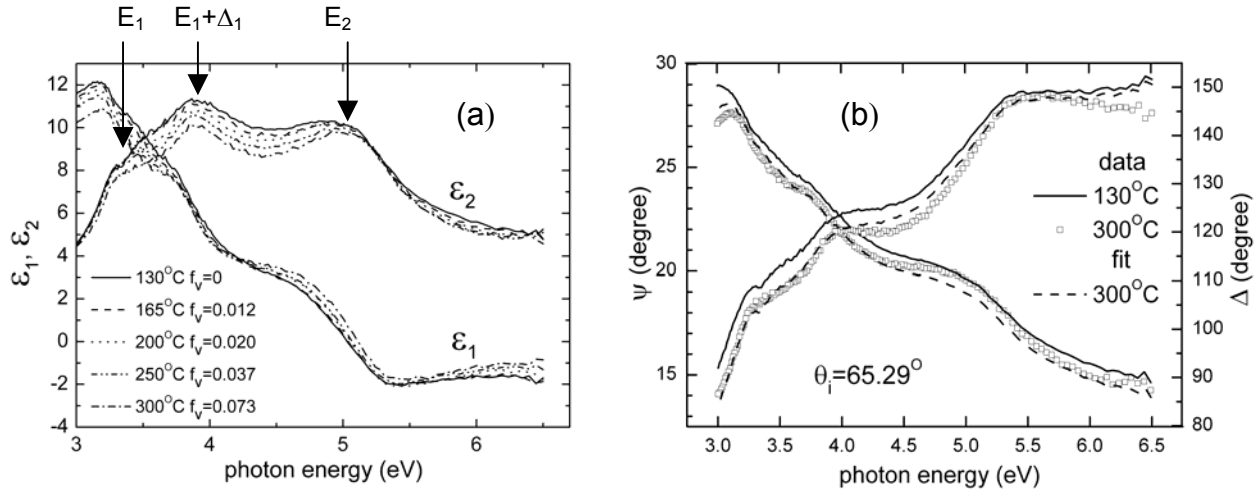

Fig. 7 (a) Dielectric functions measured at room temperature for five CdTe films deposited at different nominal substrate temperatures, as deduced from a two-layer (roughness/bulk) model of the film at a thickness of 1000 Å; (b) a representative fit to the SE data obtained at room temperature for the CdTe film deposited at 300°C, assuming a two-layer model and using the room temperature dielectric function for the film prepared at 130°C as a dense-film reference. For this analysis in (b), the void fraction relative to the film deposited at 130°C is obtained, and these results are listed in (a) for all five films.

substrate temperature. The void volume fraction values in Fig. 7(a) for each substrate temperature are obtained by using as a reference the dielectric function of the film deposited at 130°C, and then modeling the other films assuming a mixture of this densest material and void. Thus, the void contents are obtained relative to the CdTe bulk layer deposited at 130°C. Figure 7(b) shows an example of the single-parameter fit of the dielectric function of the CdTe deposited at 300°C that yields a void volume fraction of 0.073. In general, the fit is very good; however, "second order" effects other than additional voids can cause the differences in the dielectric functions in Fig. 7(a), including grain size that may narrow the peaks or grain orientation that may change the relative amplitudes of the peaks.

Figure 8 shows the evolution of the void volume fraction and the surface roughness layer thickness versus bulk layer thickness in the later stages of growth, as determined using data over the spectral range from 4 to 6.5 eV. The maximum absorption depth in this case is ~250 Å, which defines the depth resolution of the analysis. In this analysis, a single-layer model is used, representing a surface roughness layer on top of opaque CdTe with a variable void volume fraction. Because the roughness layer is such a large fraction of the penetration depth, then the void fraction in this analysis tends to be over-estimated since the information comes from the near-surface bulk material just beneath the surface roughness layer. The surface roughness layer is only approximated as a single layer, but is in fact graded from the bulk to the surface.

In spite of the expected over-estimate of the absolute magnitude of the void fraction, the trends in Fig. 8 are informative. First, for the lowest void volume fraction layers, i.e., those prepared at nominal temperatures of 130°C and 165°C, the void fraction exhibits well defined increases. Apparently the increase occurs most abruptly and at the lowest thickness when the starting void fraction is the lowest. Thus, for the 130°C deposition, the transition occurs near 1500 Å and saturates after ~2000 Å, whereas for 165°C, the transition occurs near 2000 Å and has yet to saturate by the end of the deposition. This microstructural transition is tentatively attributed to

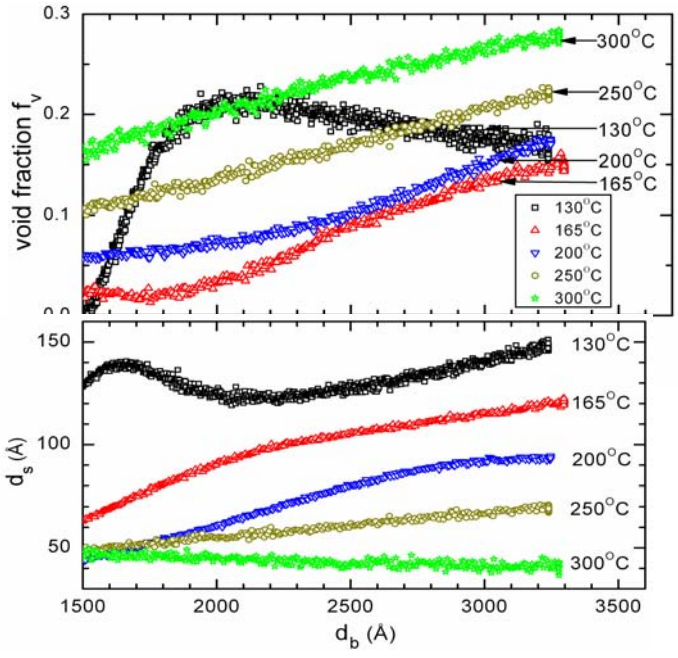

Fig. 8: Evolution of the void volume fraction and the surface roughness layer thickness for a series of five CdTe films deposited at different nominal substrate temperatures starting from a bulk layer thickness of 1500 Å and continuing to the end of deposition. The depositions at nominal temperatures of 130°C and 165°C exhibit well-defined bulk structural transitions at ~1500 Å and ~2000 Å, respectively.

the development of stress in the lowest substrate temperature materials that builds up due to a combination of ion bombardment-induced densification along with the limited surface diffusion and structural relaxation at the lower temperatures. The first indication of the onset of this transition is a super-linear increase in roughness which is clearest in Fig. 6 for the 130°C deposition. For the higher substrate temperature depositions that do not show a clear structural transition, the void fraction monotonically increases with thickness and the surface roughness increase saturates at a bulk layer thickness that decreases with increasing temperature. The standard nominal temperature chosen for sputtering CdTe for incorporation into solar cells is 200°C. This deposition temperature leads to the highest density structure while avoiding the apparent stress-induced microstructural transition.

The structural transition with thickness has also been detected in a second CdTe deposition performed on a c-Si substrate at a true substrate temperature of 130°C. For this deposition, the graphite cloth was not used between the substrate and its holder. Because the nominal and true substrate temperatures were significantly different in this case, SE calibration of the true substrate temperature was required. For this deposition, the Ar pressure and plasma power were 18 mTorr and 50 W rf plasma power. In this study, SE measurements were performed not only during growth, but also during sample etch-back using ~20 steps of Br_2-methanol etching. The analysis was performed over the photon energy range of 5.0-6.5 eV, where the absorption depth is ~100 Å or less, and final results are shown in Fig. 9. In this analysis as in Fig. 8, it is expected that the void volume fraction is over-estimated due to the close proximity of the relatively thick surface roughness layer. In spite of this problem, the results of Fig. 9 reproduce those in Fig. 8 for a different deposition, demonstrating a clear structural transition in both the growth and etching data. In particular, the structural transition is observed after a bulk layer thickness of ~1500 Å in which case the void volume fraction increases to ~0.2 as the thickness increases to 2000 Å.

In another approach, the evolution of the film structure can be obtained from the real time SE data by using the full spectral range and applying multilayer optical analysis. In this case, the film structure is built up one layer at a time in such a way as to retain a high quality of the fit to the data collected throughout the deposition. Such results are presented in Figs. 10(a) and (b) for the depositions of Figs. 8 and 9 with 130°C nominal and 130°C true substrate temperatures,

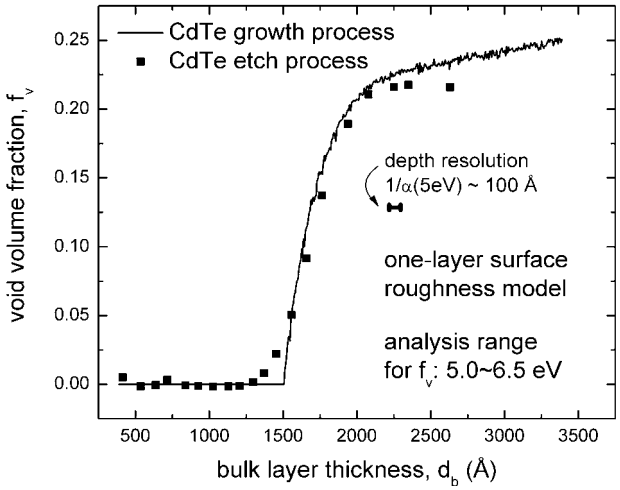

Fig. 9: Depth profiles in the void volume fraction for a CdTe film deposited on a c-Si substrate with a true substrate temperature of 130°C, obtained by real time SE during growth and by ex situ SE during etching. In the analysis, a single-layer model is used consisting of a surface roughness layer on top of opaque CdTe.

respectively. In both cases, the largest increase in void fraction occurs within the range of ~1500-2000 Å. Other characteristics of the film deduced from the different fitting procedures are similar, including the surface roughness and bulk layer thicknesses. One clear difference in the results of Fig. 10 in comparison with those of Figs. 8 and 9 is the factor of two lower void volume fraction after the transition (0.1 vs. ~0.2). This difference, which appears consistently for the two depositions, is attributed to the fact that the depth range over which averaging occurs is larger for the multilayer model and extends well below the roughness layer. In contrast, a continuous measurement of the near-surface detects surface connected voids that are associated with the surface roughness layer.

To conclude this section of the report, studies of the depth dependence of the broadening parameters associated with the optical transitions in as-deposited films have been initiated. This effort is an attempt to corroborate in the as-deposited films the results obtained in the step-wise etching studies of $CdCl_2$-treated CdTe in solar cells. These latter results were presented in the first quarter report of Phase I and showed an increase in the broadening parameters for the E_1 and E_2 transitions of CdTe with successive etching steps into the CdTe layers of the solar cells.

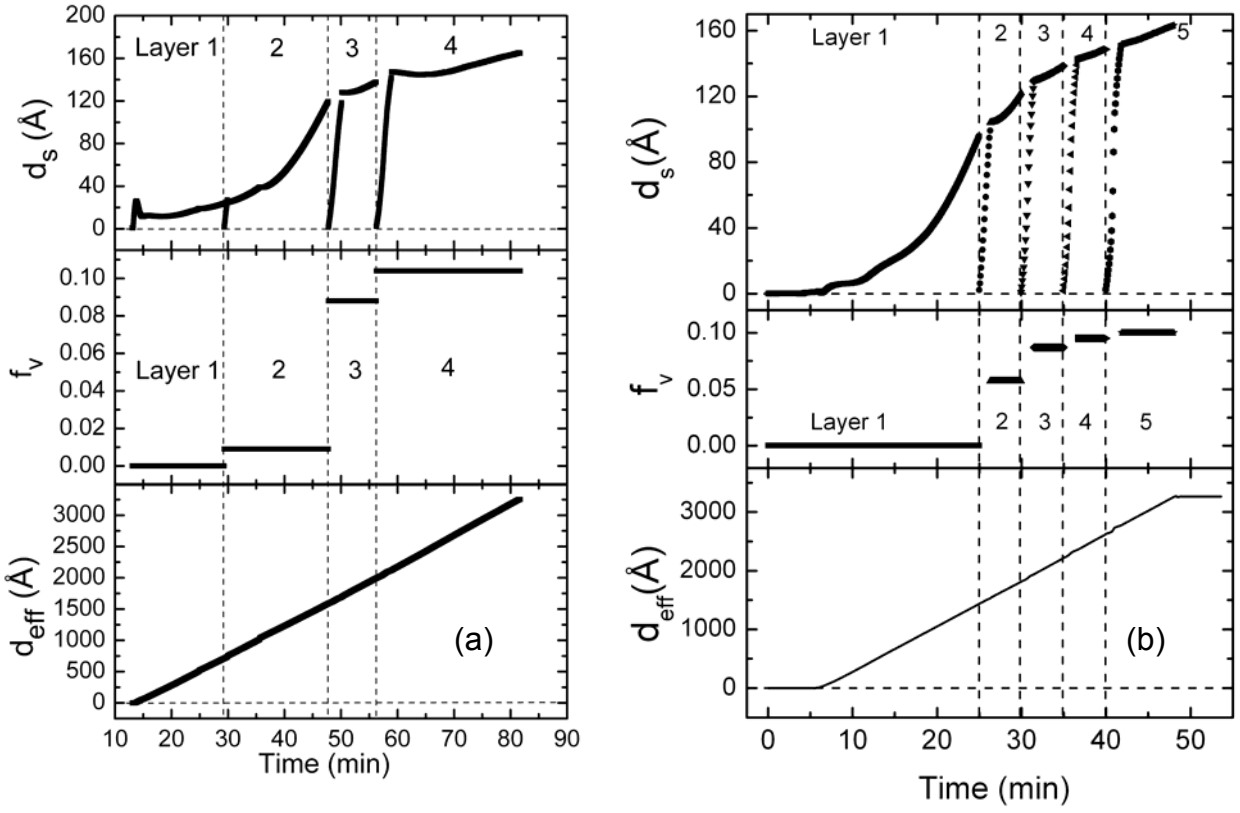

Fig. 10: Microstructural evolution deduced by real time SE for two CdTe films deposited on c-Si substrates with (a) a nominal temperature of 130°C (deposition from the series of Fig. 4) and (b) a true temperature of 130°C (deposition from Fig. 5). Included in the analyses are the (top) surface roughness layer thickness; (center) bulk layer void volume fraction; and (bottom) effective thickness (the volume of film material per unit area considering all the layers). In (a) and (b) four and five layer models for the film structure are used.

This behavior suggested that the grain size of the CdTe layers decrease with increasing depth into the material. Such behavior is an expected result of the nucleation and growth of the as-deposited thin films as well as the grain growth processes that may occur during the $CdCl_2$ treatment. To explore these effects in as-deposited CdTe, a multilayer analysis similar to that shown in Fig. 10 is performed. Rather than modeling each layer in terms of a mixture of the near-substrate material and voids as in Fig. 10, the dielectric function of the layer is determined by exact inversion. Because the optical equations are inverted exactly, all noise in the raw data are transferred to the dielectric function (see Fig. 11).

Figure 11(a) shows results for the CdTe film of Figs. 9 and 10(b), incuding the dielectric function of the dense layer in the initial stages of growth, and the lower density layer ($f_v \sim 0.1$) nearest the surface. Although the near surface layer has a higher void density, the broadening parameter associated with the fundamental gap E_0 has decreased measurably (from Γ_0=0.156 eV to 0.142 eV), indicating an increase in grain size with increasing accumulated thickness. This appears to be related to the same effects observed for the E_1 and E_2 transitions of the CdTe in the solar cell configuration. In this configuration, however, it is too difficult to extract the dielectric function near E_0 due to the superposition of a complex interference structure. In contrast, in Fig. 11(a) it is more difficult to extract accurate values of the E_1 and E_2 broadening parameters due to the presence of thick surface roughness layers on the growing film. For the solar cell studies, the effect of the Br_2-methanol etching treatment is to reduce this thickness to 20-40 Å, significantly lower than that on the final as-deposited CdTe film. Finally, Fig. 11(b) shows corresponding results for a CdS film deposited under conditions used for superstrate solar cells, but on a c-Si substrate. These include a nominal temperature of 200°C, an Ar pressure of 10 mTorr, and a plasma power of 50 W. This film shows an even larger difference between the substrate interface (Γ_0=0.287 eV) and the near-surface (Γ_0=0.131 eV) CdS materials. Thus, more

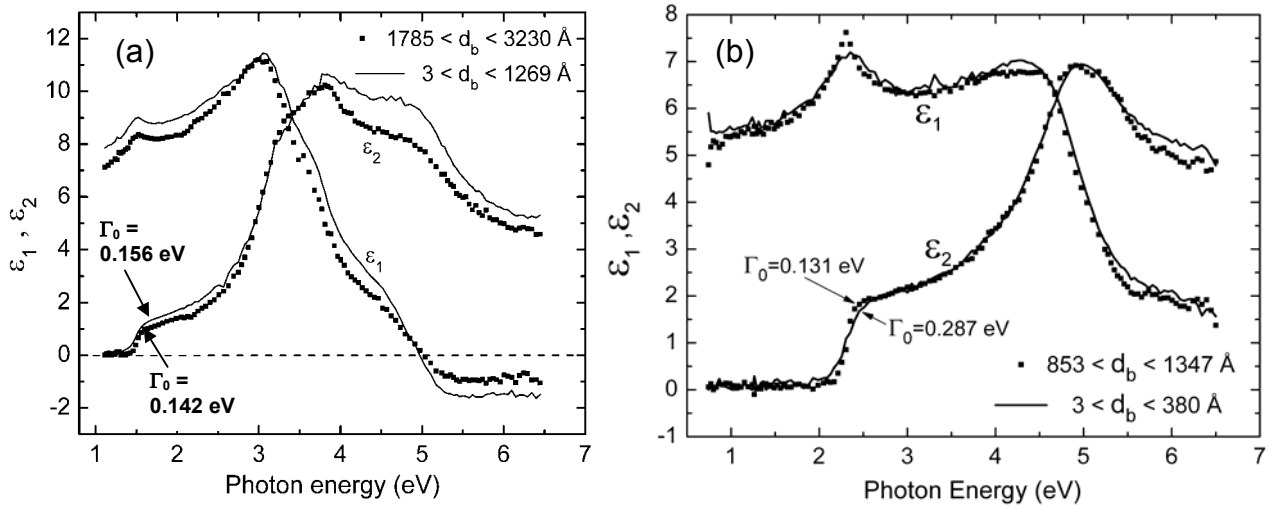

Fig. 11: Dielectric functions for (a) CdTe and (b) CdS deposited on c-Si wafer substrates that are characteristic of the material near the substrate interface (solid lines) and near the surface of the film (points). Highlighted here are the widths of the E_0 critical points, obtained in best fits using the critical-point parabolic-band approximation.

significant grain coarsening is built into an even thinner layer in the case of CdS. The grain size evolution characterized here in CdTe and CdS will be studied in greater detail later in Phase I as a function of substrate (selecting device relevant substrates) and as a function of preparation parameters.

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